

IN THE CLAIMS:

The current claims follow. For claims not marked as amended in this response, any difference in the claims below and the previous state of the claims is unintentional and in the nature of a typographical error.

1. (Currently Amended) A circuit comprising a first and a second circuit module and a synchronization module the first and the second module being mutually ~~a-synchronous~~ asynchronous, and being coupled by the synchronization module, the synchronization module comprising

a transfer register for storing data which is communicated between the two circuit modules,
a control circuit for controlling the register in response to a respective timing signal (~~St1, St2~~) from the first and the second circuit module, the control circuit comprising a control chain for generating a control signal (~~CR~~) for the transfer register the control chain including at least

- a repeater for inducing changes in the value of the control signal,
- ~~at least~~ one edge sensitive element for delaying a change in the signal value until a transition in a selected one of the timing signals is detected.

2. (Currently Amended) A circuit according to claim 1, further comprising a comparator for generating a difference signal (~~AD~~) upon detection of a difference between an input and an output of the transfer register the control chain further comprising a wait element for delaying an active transition in the control signal until a difference is detected.

3. (Previously Presented) A circuit according to claim 1 wherein the control chain further comprises an arbitration element the arbitration element having respective channels for guiding at least a first and a second signal flow, the arbitration element being arranged for arbitrating between passing active events in the first and the second signal flow, the first channel being arranged between an output of the edge sensitive element and an input of the repeater.

4. (Currently Amended) A circuit according to claim 3, wherein the selected timing signal is a clock signal (~~Wclk~~) from the first circuit module wherein the timing signal from the second circuit module is an access request signal (~~Rreq~~), the second channel of the arbitration element having a first input for receiving the access request signal (~~Rreq~~) and a first output for providing an access acknowledge signal (~~Rack~~) to the second circuit module.

5. (Currently Amended) A circuit according to claim 3, further comprising an auxiliary register for transferring data from the first module to the register wherein the selected timing signal is a clock signal (~~Rclk~~) from the second circuit module wherein the timing signal from the first circuit module is a write request signal (~~Wreq~~), the second channel of the arbitration element having a second input (~~e~~) for receiving the write request signal and a second output (~~d~~) for providing a control signal to control the auxiliary register.

6. (Currently Amended) A circuit according to claim 1 wherein the selected one of the timing signals is a clock signal (~~Wclk~~) from the first circuit module the circuit including an auxiliary register for transferring data from the transfer register to the second circuit module and wherein the circuit includes a further edge sensitive element for delaying a change in a control signal for the auxiliary register until a transition is detected in a timing signal (~~Relk~~) from the second circuit module.

7. (Previously Presented) A circuit according to claim 6, wherein the further edge sensitive element is part of the control chain.

8. (Previously Presented) A circuit according to claim 6, wherein the further edge sensitive element is part of a further control chain, which is coupled to the control chain.

9. (Previously Presented) A circuit according to claim 1, wherein the synchronization module has a first transfer register for transferring data from the first to the second circuit module and a second transfer register for transferring data from the second to the first circuit module the transfer registers being controlled by the same control signal.

10. (Currently Amended) A method for transferring data between a first and a second circuit module using a synchronization module the first and the second module being mutually ~~a-~~ ~~synelwoneous~~, asynchronous and being coupled by the synchronization module, the method comprising the following steps

- temporarily storing data which is transferred from the first to the second circuit module in a register,

- controlling the register in response to a respective timing signal from the first, and the second circuit module, by a control circuit which comprises a control chain for generating a control signal wherein

- changes are induced in the value of the control signal,
- a change in the control signal value is delayed until a transition in a selected one of the timing signals is detected.